REMARKS

Claim 1-154 are pending. In this Response, claims 1, 11, 21, 61, 76 and 141 have been amended, and claims 151-154 have been added.

I. DRAWING/SPECIFICATION OBJECTIONS

The Drawings and the Specification are objected to under 37 C.F.R. § 1.84(p)(4) due to an improper reference character.

The Examiner asserts that reference character 144 has been used to designate both a photoresist layer and a metal trace. Applicant agrees. Accordingly, the Drawings and the Specification have been amended to designate the photoresist layer with reference character 143 (rather than 144).

Therefore, Applicant requests that these objections be withdrawn.

II. SECTION 102 REJECTIONS – YAMANAKA

Claims 1, 3-9, 21, 23-29, 61, 63, 66, 68, 71, 73, 91, 93, 96, 98, 101, 103, 106, 108, 111, 113, 116 and 118 are rejected under 35 U.S.C. § 102(b) as being anticipated by *Yamanaka* (U.S. Patent No. 5,893,723).

Yamanaka discloses semiconductor unit 10 that includes lead frame 3, base portion 5, frame portion 6, semiconductor device 7, bonding wire 8, translucent resin 9, insulating paste 71 and thin film 91. Lead frame 3 includes inner lead portion 31 and outer lead portion 32. Base portion 5 includes recessed portion 51.

Yamanaka also discloses a manufacturing method for the semiconductor unit that reduces camber of the base portion and enhances reliability in operation.

> An object of the present invention is to provide a manufacturing method for a semiconductor unit which is capable of reducing camber of a base portion and enhancing reliability in operation. (Col. 2, lines 20-23.) (Emphasis added.)

Upper mold 1 and lower mold 2 clamp and hold lead frame 3 so as to hold outer lead portion 31 therebetween and position inner lead portion 32 in cavity 4 (Fig. 1A). Thereafter, resin is injected into cavity 4 to form base portion 5 and frame portion 6 (Fig. 1B). Next, a trim and form operation cuts outer lead portion 31 into the desired length and then folds outer lead portion 31 into a specified shape (Fig. 1C).

Semiconductor device 7 is then mounted in recessed portion 51 through insulating paste 71, and then semiconductor device 7 is connected to inner lead portion 32 by bonding wire 8 (Fig. 2A). Next, translucent resin 9 is potted in recessed portion 51, thereby sealing semiconductor device 7 and bonding wire 8 (Fig. 2B). Finally, thin film 91 is coated on translucent resin 9 (Fig. 3).

Yamanaka describes mounting semiconductor device 7 in recessed portion 51 as follows:

> After trim and forming of the outer lead portion 31, a semiconductor device 7 is mounted, as shown in FIG. 2A. The semiconductor device 7 is mounted in the recessed portion 51 of the base portion 5 through insulating paste 71. In this case, the insulating paste 71 and the like are hardened by curing at a temperature of 150° C. for one hour. In this mounting, since the camber of base portion 5 is very small, the semiconductor device 7 can be certainly mounted at an accurate position. In particular, this is effective for a semiconductor unit such as a CCD linear sensor in which a long-size semiconductor device 7 is mounted. (Col. 5, lines 48-58.) (Emphasis added.)

Yamanaka fails to teach or suggest that semiconductor device 7 contacts base portion 5. Instead, *Yamanaka* discloses that semiconductor device 7 is mounted on base portion 5 using insulating paste 71. Furthermore, *Yamanaka* shows insulating paste 71 contacts the outer side surfaces of semiconductor device 7 and tapers with thickness that decreases as the lateral distance from semiconductor device 7 increases.

Those skilled in the art would understand that insulating paste 71 is deposited on base portion 5 in non-solidified form, then semiconductor device 7 is inserted into insulating paste 71, thereby squeezing insulating paste 71 between base portion 5 and semiconductor device 7 outwardly and increasing the thickness of insulating paste 71 at the outer side surfaces of

semiconductor device 7, and then insulating paste 71 is cured so that semiconductor device 7 is "certainly mounted at an accurate position."

Those skilled in the art would also understand that insulating paste 71 contacts and is sandwiched between base portion 5 and semiconductor device 7, and base portion 5 and semiconductor device 7 are spaced and separated from one another after insulating paste 71 is cured. In other words, those skilled in the art would understand that base portion 5 does not contact semiconductor device 7. That is, inserting semiconductor device 7 into insulating paste 71 would not displace all insulating paste 71 between base portion 5 and semiconductor device 7. Instead, a thin film of insulating paste 71 would remain intact between base portion 5 and semiconductor device 7, as is conventional with die attach.

Those skilled in the art would find this readily apparent for several reasons.

First, inserting semiconductor device 7 into insulating paste 71 with sufficient pressure to contact base portion 5 and semiconductor device 7 is probably impossible. Base portion 5 is formed with a resin that prevents camber, and semiconductor device 7 is mounted over a flat surface in recessed portion 51. As a result, insulating paste 71 probably remains embedded between base portion 5 and semiconductor device 7 regardless of how much pressure is applied when semiconductor device 7 is inserted into insulating paste 71.

Second, even if inserting semiconductor device 7 into insulating paste 71 could contact base portion 5 and semiconductor device 7 (which is extremely unlikely), the large pressure needed to do so would probably damage semiconductor device 7. Those skilled in the art would not infer that *Yamanaka* teaches this approach, particularly since *Yamanaka* seeks to enhance reliability.

Third, even if inserting semiconductor device 7 into insulating paste 71 could contact base portion 5 and semiconductor device 7 (which is extremely unlikely), the contact area between base portion 5 and insulating paste 71, and between semiconductor device 7 and insulating paste 71, would diminish. Those skilled in the art would not infer that *Yamanaka* teaches this approach, particularly since *Yamanaka* seeks to certainly mount semiconductor device 7 in an accurate position.

Fourth, *Yamanaka* says nothing about base portion 5 contacting semiconductor device 7.

Fifth, those skilled in the art would recognize that although insulating paste 71 is not shown between base portion 5 and semiconductor device 7 in the drawings, this does not convey that base portion 5 contacts semiconductor device 7. Instead, this conveys that the drawings were simplified by omitting a relatively unimportant detail. This is especially clear given the overall simplicity of the drawings. For instance, semiconductor device 7 is shown as a unitary structure without a conductive pad, however those skilled in the art would recognize that semiconductor device 7 must include a conductive pad that contacts bonding wire 8. Although the conductive pad (like insulating paste 71 between base portion 5 and semiconductor device 7) is omitted in the drawings, its presence would be abundantly clear to those skilled in the art, regardless of whether it is shown.

Claim 1 recites "a first single-piece non-transparent insulative housing portion that contacts the lower surface [of the chip]," claims 21, 91, 96, 101, 106, 111 and 116 recite "the first housing portion is a single-piece that contacts the chip" and claims 61, 66 and 71 recite "a first single-piece non-transparent insulative housing portion that contacts the chip."

Yamanaka fails to teach or suggest this approach. Base portion 5 does not contact semiconductor device 7.

In sustaining this rejection, the Examiner asserts that "insulative housing portion (5) contacts the chip."

Applicant disagrees. The Examiner has misconstrued *Yamanaka*, as mentioned above.

Moreover, the Examiner asserts that semiconductor device 7 includes "a conductive pad (between the chip and a wire 8)" thereby inferring an apparent feature that is not explicitly disclosed for the purpose of rejecting the claims, but on the other hand, asserts that "insulative housing portion (5) contacts the chip" thereby ignoring an apparent feature that is not explicitly disclosed for the purpose of rejecting the claims. The Examiner's treatment of these apparent features is inconsistent and it is improper and unfair for the Examiner to adopt this tactic.

Under 35 U.S.C. § 102, anticipation requires that each and every element of the claimed invention be disclosed in the prior art. *Akzo N.V. v. United States International Trade Commission*, 1 USPQ 2d 1241, 1245 (Fed. Cir. 1986), *cert. denied*, 482 U.S. 909 (1987). That is, the reference must teach every aspect of the claimed invention. See M.P.E.P. § 706.02.

Yamanaka fails to teach or suggest limitations of independent claims 1, 21, 61, 66, 71, 91, 96, 101, 106, 111 and 116. Therefore, Applicant requests that these rejections be withdrawn.

III. SECTION 102 REJECTIONS – NAKAMURA ET AL.

Claims 1-5, 7-13, 15-23, 25-30, 61, 62, 65, 76, 77, 80, 141-143 and 145 are rejected under 35 U.S.C. § 102(b) as being anticipated by *Nakamura et al.* (U.S. Patent No. 5,405,809).

Nakamura et al. discloses an image sensor device that includes light-transmitting substrate 21, circuit conductor layer 22, plated metal layer 23, metal bump 24, image sensor chip 26, resin coating 27 and transparent resin 28. Image sensor chip 26 includes electrode 25 and light-sensitive element 29.

Metal bump 24 is a metal such as Au that is formed on electrode 25 by plating or ball bonding, and then image sensor chip 26 is cut out from a silicon wafer.

Circuit conductor layer 22 is a metal such as Cu or Al that is formed on light-transmitting substrate 21. For instance, circuit conductor layer 22 may be formed by depositing a metal layer on light-transmitting substrate 21 by sputtering, vapor deposition and the like and then patterning the metal layer using photolithography. Alternatively, circuit conductive layer 22 may be formed by attaching a flexible printed wiring board to light-transmitting substrate 21 or by thick-film printing.

Plated metal layer 23 is then formed on a prescribed portion of circuit conductor layer 22.

Transparent resin 28 is then applied to a prescribed portion of light-transmitting substrate 21, and then image sensor chip 26 is disposed face-down on transparent resin 28 so that plated metal layer 23 abuts electrode 25. While image sensor chip 26 is pressed onto light-transmitting

substrate 21, transparent resin 28 is irradiated with ultra violet rays through light-transmitting substrate 21 and partially cured.

The structure is then placed in an oven that melts plated metal layer 23 and further cures transparent resin 28. Plated metal layer 23 melts and recoagulates so that alloy layers are formed in abutting portions between circuit conductor layer 22 and plated metal layer 23, and in abutting portions between plated metal layer 23 and metal bump 24.

Finally, resin coating 27 such as silicon is dispensed on light-transmitting substrate 21 and image sensor chip 26.

Claims 1-5 and 7-10

Claim 1 recites "the first housing portion includes a peripheral ledge, and the second housing portion is exposed within the peripheral ledge." *Nakamura et al.* fails to teach or suggest this approach. Light-transmitting substrate 21 is not within a peripheral ledge of resin coating 27, and transparent resin 28 is not exposed.

In sustaining this rejection, the Examiner asserts that "a second transparent insulative housing portion (21 and 28) . . . is located within the peripheral ledge . . . and portion (21) is exposed."

Applicant disagrees. Light-transmitting substrate 21 is not located within a peripheral ledge of resin coating 27. However, in the interests of expediting the case, claim 1 has been amended to recite that the second housing portion is "exposed" within the peripheral ledge thereby rendering this rejection moot.

Claims 11-13, 15-20, 61, 62 and 65

Claim 11 recites "a conductive trace that extends laterally through an opening in the first housing portion . . . wherein the first housing portion spans 360 degrees around the conductive trace at the opening ." Claim 61 recites similar limitations. *Nakamura et al.* fails to teach or suggest this approach. Circuit conductor layer 22 does not extend through an opening in resin

coating 27, much less extend laterally through the opening such that resin coating 27 spans 360 degrees around circuit conductor layer 22 at an opening.

In sustaining this rejection, the Examiner does not even attempt to explain how circuit conductor layer 22 extends through an opening in resin coating 27.

However, in the interests of expediting the case, claims 11 and 61 have been amended to recite that the conductive trace extends "laterally" through an opening in the first housing portion such that "the first housing portion spans 360 degrees around the conductive trace at the opening" thereby rendering this rejection moot.

Claims 21-23, 25-30, 141-143 and 145

Claim 21 recites "the first housing portion . . . provides the peripheral side surfaces . . . and the second housing portion . . . does not extend across any of the peripheral side surfaces . . . is transparent and is exposed." Claim 141 recites similar limitations. *Nakamura et al.* fails to teach or suggest this approach. Light-transmitting substrate 21 extends across the peripheral side surfaces of resin coating 27, and transparent resin 28 is not exposed.

In sustaining this rejection, the Examiner asserts that "insulative housing (27) has flat ('uncurved') peripheral side surfaces at least at the center portion of the sides."

Applicant disagrees. Resin coating 27 has curved peripheral side surfaces. However, in the interests of expediting the case, claims 21 and 141 have been amended to recite that the second housing portion "does not extend across any of the peripheral side surfaces" and is "exposed" thereby rendering this rejection moot.

Claims 76, 77 and 80

Claim 76 recites "a conductive trace that includes a lead and a planar metal trace, wherein the lead extends through an opening in the first housing portion, extends outside the insulative housing, does not extend across any edge of the pad and is electrically connected to the pad inside the insulative housing, and the planar metal trace contacts and is not integral with the lead, contacts the first housing portion, extends across one of the side surfaces and does not extend

outside the insulative housing." *Nakamura et al.* fails to teach or suggest this approach. Circuit conductor layer 22 extends across electrode 25, circuit conductor layer 22 does not extend through an opening in resin coating 27, and plated metal layer 23 does not extend across a side surface of image sensor chip 26.

In sustaining this rejection, the Examiner asserts that "Nakamura et al. discloses . . . a conductive trace (22 and 23) that includes a lead (22) and a planar metal trace (23 . . .), wherein the lead extending through an opening in the first housing portion . . . and the planar metal trace . . . extending across one of the side surfaces."

Applicant disagrees. Circuit conductor layer 22 does not extend through an opening in resin coating 27, and plated metal layer 23 does not extend across a side surface of image sensor chip 26. However, in the interests of expediting the case, claim 76 has been amended to recite that the lead "does not extend across any edge of the pad" thereby rendering this rejection moot.

Claims 1-5, 7-13, 15-23, 25-30, 61, 62, 65, 76, 77, 80, 141-143 and 145

Under 35 U.S.C. § 102, anticipation requires that each and every element of the claimed invention be disclosed in the prior art. *Akzo N.V. v. United States International Trade Commission*, 1 USPQ 2d 1241, 1245 (Fed. Cir. 1986), *cert. denied*, 482 U.S. 909 (1987). That is, the reference must teach every aspect of the claimed invention. See M.P.E.P. § 706.02.

Nakamura et al. fails to teach or suggest limitations of independent claims 1, 11, 21, 61, 76 and 141. Therefore, Applicant requests that these rejections be withdrawn.

IV. SECTION 103 REJECTIONS

Claims 10, 30, 65, 70, 75, 76, 78, 80, 81, 83, 85, 86, 88, 90, 95, 100, 105, 110, 115 and 120 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yamanaka* in view of *Tsuji* (U.S. Patent No. 5,530,282).

Tsuji discloses a semiconductor device that includes die pad 2, inner lead 3, semiconductor element 4, mold 8 and bridge structure 10. Semiconductor element 4 includes bond pad 5 and bump 6. Bridge structure 10 includes insulating film 11 and conductive thin film pattern 12. Bridge structure 10 electrically connects inner lead 3 and bump 6.

Claims 10, 30, 65, 70, 75, 95, 100, 105, 110, 115 and 120

Claims 10, 30, 65, 70, 75, 95, 100, 105, 110, 115 and 120 depend from claims 1, 21, 61, 66, 71, 91, 96, 101, 106, 111 and 116, respectively.

In sustaining this rejection, the Examiner asserts that "Yamanaka discloses the claimed invention except for the device having a planar trace and being devoid of wire bonds, TAB leads and solder joints."

Yamanaka fails to teach or suggest limitations of claims 1, 21, 61, 66, 71, 91, 96, 101, 106, 111 and 116, as mentioned above.

Claims 76, 78, 80, 81, 83, 85, 86, 88 and 90

Claim 76 recites "the planar metal trace . . . contacts the first housing portion." Claims 81 and 86 recite similar limitations. *Yamanaka* fails to teach or suggest this approach. Bonding wire 8 does not contact base portion 5. *Tsuji* fails to cure this deficiency. Even if bridge structure 10 was used instead of bonding wire 8, bridge structure 10 would not contact base portion 5.

In sustaining this rejection, the Examiner asserts that "Yamanaka discloses the claimed invention except for the device having a planar trace and being devoid of wire bonds, TAB leads and solder joints."

Applicant disagrees. The Examiner has misconstrued *Yamanaka*, as mentioned above.

Claims 10, 30, 65, 70, 75, 76, 78, 80, 81, 83, 85, 86, 88, 90, 95, 100, 105, 110, 115 and 120

Yamanaka in view of *Tsuji* fails to teach or suggest limitations of independent claims 1, 21, 61, 66, 71, 76, 81, 86, 91, 96, 101, 106, 111 and 116. Therefore, Applicant requests that these rejections be withdrawn.

V. CLAIM OBJECTIONS

Claims 14, 64, 67, 69, 72, 74, 79, 82, 84, 87, 89, 92, 94, 97, 99, 102, 104, 107, 109, 112, 114, 117, 119 and 144 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all limitations of the base claim and any intervening claims.

Claim 151 constitutes claim 14 rewritten in independent form including all limitations of the base claim and any intervening claims.

Claim 152 constitutes claim 64 rewritten in independent form including all limitations of the base claim and any intervening claims.

Claim 153 constitutes claim 79 rewritten in independent form including all limitations of the base claim and any intervening claims.

Claim 154 constitutes claim 144 rewritten in independent form including all limitations of the base claim and any intervening claims.

VI. DRAWING AMENDMENTS

The Drawings have been amended at Figs. 2A, 2C, 2F, 6B, 6D, 7D, 8A, 8B, 9A, 9B, 10A, 10B, 10C, 11A, 11B, 12A, 12B, 13B and 14B to improve clarity. No new matter has been added.

The Appendix with amended drawing figures is attached hereto. The Appendix includes a Replacement Sheet and an Annotated Sheet Showing Changes for each amended figure.

Fig. 2A

Metal base 120 is shown in Figs. 2A and 2B. Metal base 120 includes surfaces 122 and 124, central portion 126, slots 128, recessed portions 132 and 134, non-recessed portions 136 and leads 138. Recessed portions 132 are formed in surface 124 between slots 128, non-recessed portions 136 are formed between slots 128, and leads 138 include recessed portions 132 and non-recessed portions 136.

In Fig. 2A as amended, reference character 132 has a straighter lead line.

Figs. 2C and 2F

Photoresist layers 142 and 144 are formed on surfaces 122 and 124, respectively, in Figs. 2C and 2F. Metal traces 144 are formed on metal base 120 in Figs. 3A and 3B. Thus, reference character 144 is used twice.

In Figs. 2C and 2F as amended, photoresist layer 143 (rather than 144) is formed on surface 124.

Fig. 6B

Encapsulant 156 is formed on chip 110 and metal base 120 and fills slots 128 and recessed portions 132 and 134 in Figs. 6A and 6B. Encapsulant 156 includes bottom surface 160, peripheral side surfaces 162, top surface 164 and peripheral portion 166

In Fig. 6B as amended, reference character 156 points to encapsulant 156 rather than lead 138, as would be apparent to those skilled in the art.

Figs. 6D and 7D

Leads 138 extend outwardly from central portion 126 between slots 128 and include recessed portions 132 and non-recessed portions 136 in Figs. 2A and 2B.

Metal traces 144 are formed on metal base 120 in Figs. 3A and 3B. Metal traces 144 extend from central portion 126 to recessed portions 132. Conductive traces 150 include leads 138 and metal traces 144.

Transparent adhesive 154 is formed on metal base 120 and metal traces 144 in Figs. 4A and 4B.

Chip 110 is mechanically attached to metal base 120 using transparent adhesive 154 in Figs. 5A and 5B. Leads 138 are outside the periphery of chip 110 as shown in Fig. 5A.

Encapsulant 156 is formed on chip 110 and metal base 120 and fills slots 128 and recessed portions 132 and 134 in Figs. 6A and 6B.

Encapsulant 156 is removed from laterally extending portions of slots 128 in Figs. 7A and 7B.

Figs. 2F, 2G and 2H are enlarged cross-sectional views showing the formation of recessed portion 132 taken across line 2F—2F in Figs. 2A and 2B, Figs. 3C, 3D and 3E are enlarged cross-sectional views showing the formation of metal trace 144 taken across line 3C—3C in Fig. 3A, Fig. 4C is an enlarged cross-sectional view showing transparent adhesive 154 taken across line 4C—4C in Fig. 4A, Fig. 6D is an enlarged cross-sectional view showing encapsulant 156 taken across line 6D—6D in Fig. 6A, and Fig. 7D is an enlarged cross-sectional view showing encapsulant 156 taken across line 7D—7D in Fig. 7A.

Although metal trace 144 is not labeled in Figs. 6D and 7D, its identification is clear from Fig. 3D.

In Figs. 6D and 7D as amended, metal trace 144 is labeled, as would be apparent to those skilled in the art.

Figs. 8A, 8B, 9A, 9B, 10A, 10B, 11A, 11B, 12A and 12B

Protective coating 170 is formed on metal base 120 outside encapsulant 156 in Figs. 8A and 8B. Protective coating covers the exposed surfaces of metal base 120 outside central portion 126 of metal base 120, and central portion 126 remains exposed. Protective coating 170 is considered a surface layer that is part of metal base 120 and leads 138.

In Figs. 8A, 8B, 9A, 9B, 10A, 10B, 11A, 11B, 12A and 12B as amended, the lines between leads 138 and the rectangular peripheral frame of metal base 120 are removed so that Figs. 8A, 8B, 9A, 9B, 10A, 10B, 11A, 11B, 12A and 12B are consistent with Figs. 7A and 7B, as would be apparent to those skilled in the art.

In Figs. 8B, 9B, 10B, 11B and 12B as amended, the lines between the portion of metal base 120 that protrudes from the opposing narrow side surfaces 162 of encapsulant 156 and the rectangular peripheral frame of metal base 120 are removed so that Figs. 8B, 9B, 10B, 11B and 12B are consistent with Fig. 7B, as would be apparent to those skilled in the art.

In Fig. 8B as amended, the lines in metal base 120 that protrude from the opposing narrow side surfaces 162 of encapsulant 156 are removed so that Fig. 8B is consistent with Fig. 7B, as would be apparent to those skilled in the art.

Figs. 9B, 10B, 11B and 12B

Central portion 126 of metal base 120 is removed thereby exposing metal traces 144 and transparent adhesive 154 in Figs. 9A and 9B. Central portion 126 is removed by a wet chemical etch that has no appreciable effect on protective coating 170. Thus, metal base 120 outside encapsulant 156 remains intact. In particular, the four portions of metal base 120 adjacent to the opposing narrow side surfaces 162 of encapsulant 156 and parallel to leads 138 remain intact as shown in Fig. 9A.

Openings 176 are formed in transparent adhesive 154 that expose pads 116 in Figs. 10A and 10B.

Connection joints 180 are formed in openings 176 that contact and electrically connect pads 116 and metal traces 144 in Figs. 11A and 11B.

Transparent base 182 is formed within peripheral portion 166 of encapsulant 156 in Figs. 12A and 12B. Encapsulant 156 and insulative base 182 in combination form insulative housing 184.

In Figs. 9B, 10B, 11B and 12B as amended, the four portions of metal base 120 adjacent to the opposing narrow side surfaces 162 of encapsulant 156 and parallel to leads 138 are shown and the various lines they cover or eliminate are removed so that Figs. 9B, 10B, 11B and 12B are consistent with Fig. 8B and with Figs. 9A, 10A, 11A and 12A, respectively, as would be apparent to those skilled in the art.

Fig. 10C

Chip 110 is mechanically attached to metal base 120 using transparent adhesive 154 such that metal traces 144 overlap and are electrically isolated from pads 116, and transparent adhesive 154 contacts and is sandwiched between metal traces 144 and pads 116 in Figs. 5A and 5B. Metal trace 144 includes a distal end that overlaps pad 116 as shown in Fig. 5C.

Openings 176 are formed in transparent adhesive 154 that expose pads 116 in Figs. 10A and 10B. Openings 176 are formed using projection laser ablation. The laser removes portions of transparent adhesive 154 above pads 116 outside metal traces 144. However, metal traces 144 shield the underlying transparent adhesive 154 from the laser etch so that the portions of transparent adhesive 154 sandwiched between metal traces 144 and pads 116 remain intact.

Fig. 10C is an enlarged perspective view of encircled detail 10C in Fig. 10B that shows pad 116, metal trace 144 and opening 176 in greater detail, and Figs. 10D and 10E are enlarged cross-sectional views taken across lines 10D—10D and 10E—10E, respectively, in Fig. 10C. Transparent adhesive 154 is shown between metal trace 144 and pad 116 in Figs. 10D and 10E.

In Fig. 10C as amended, transparent adhesive 154 is shown between metal trace 144 and pad 116, as would be apparent to those skilled in the art.

Figs. 13B and 14B

Optoelectronic semiconductor package device 186 is singulated from the lead frame in Figs. 13A and 13B. Metal base 120 is selectively cut to remove all portions of metal base 120 except for leads 138 outside insulative housing 184. This can be accomplished using an excise blade that selectively cuts metal base 120 at predetermined regions adjacent to leads 138 and insulative housing 184. Thus, metal base 120 at the opposing narrow side surfaces 162 of encapsulant 156 laterally extends to peripheral portion 166 of encapsulant 156 as shown in Fig. 13A.

Leads 138 are bent in Figs. 14A and 14B.

In Figs. 13B and 14B as amended, metal base 120 at the narrow side surface 162 of encapsulant 156 laterally extends to peripheral portion 166 of encapsulant 156 so that Figs. 13B and 14B are consistent with Figs. 13A and 14A, respectively, as would be apparent to those skilled in the art.

VII. INTERVIEW

The undersigned attorney conducted a telephone interview with Examiner Baumeister on January 2, 2004 to discuss the issues in the case, and Examiner Baumeister indicated that (1) the Section 102 rejections based *Yamanaka* would be withdrawn, (2) the Section 102 rejections based *Nakamura et al.* would likely be withdrawn, and (3) the finality of the outstanding Office Action would be withdrawn and prosecution would be reopened to permit further consideration of the amendments herein.

Applicant wishes to thank Examiner Baumeister for his courtesy and cooperation.

VIII. FEES

The fee for this Response is calculated below:

For	Claims Remaining After Amendment	Highest Number Previously Paid For		Extra Claims	Rate		Additional Fee
Total Claims	154	– 150	=	4	x $9	=	$36
Independent Claims	28	– 24	=	4	x $43	=	$172
Multiple Dep. Claim	0	0	$145			=	0
Total Fee						=	$208

Please charge the $208 to Deposit Account No. 502178/BDG005-3 and charge any underpayment or credit any overpayment to this Account.

IX. CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 2, 2004.

D Sigmond — 1/2/04

David M. Sigmond
Attorney for Applicant

Date of Signature

Respectfully submitted,

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